



PBSS4350SPN

50 V, 2.7 A NPN/PNP low V_{CEsat} (BISS) transistor

Rev. 01 — 5 April 2007

Product data sheet

1. Product profile

1.1 General description

NPN/PNP double low V_{CEsat} Breakthrough In Small Signal (BISS) transistor in a medium power Surface-Mounted Device (SMD) plastic package.

Table 1. Product overview

Type number	Package		NPN/NPN complement	PNP/PNP complement
	Nexperia	Name		
PBSS4350SPN	SOT96-1	SO8	PBSS4350SS	PBSS5350SS

1.2 Features

- Low collector-emitter saturation voltage V_{CEsat}
- High collector current capability I_C and I_{CM}
- High collector current gain (h_{FE}) at high I_C
- High efficiency due to less heat generation
- Smaller required Printed-Circuit Board (PCB) area than for conventional transistors

1.3 Applications

- Complementary MOSFET driver
- Half and full bridge motor drivers
- Dual low power switches (e.g. motors, fans)
- Automotive

1.4 Quick reference data

Table 2. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TR1; NPN low V_{CEsat} transistor						
V_{CEO}	collector-emitter voltage	open base	-	-	50	V
I_C	collector current		-	-	2.7	A
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms	-	-	5	A
R_{CEsat}	collector-emitter saturation resistance	$I_C = 2$ A; $I_B = 200$ mA	[1] -	90	130	m Ω

Table 2. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
TR2; PNP low V_{CEsat} transistor							
V_{CEO}	collector-emitter voltage	open base	-	-	-50	V	
I_C	collector current		-	-	-2.7	A	
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms	-	-	-5	A	
R_{CEsat}	collector-emitter saturation resistance	$I_C = -2$ A; $I_B = -200$ mA	[1]	-	95	140	$m\Omega$

[1] Pulse test: $t_p \leq 300$ μ s; $\delta \leq 0.02$.

2. Pinning information

Table 3. Pinning

Pin	Description	Simplified outline	Symbol
1	emitter TR1		
2	base TR1		
3	emitter TR2		
4	base TR2		
5	collector TR2		
6	collector TR2		
7	collector TR1		
8	collector TR1		

3. Ordering information

Table 4. Ordering information

Type number	Package		Version
	Name	Description	
PBSS4350SPN	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

4. Marking

Table 5. Marking codes

Type number	Marking code
PBSS4350SPN	4350SPN

5. Limiting values

Table 6. Limiting values

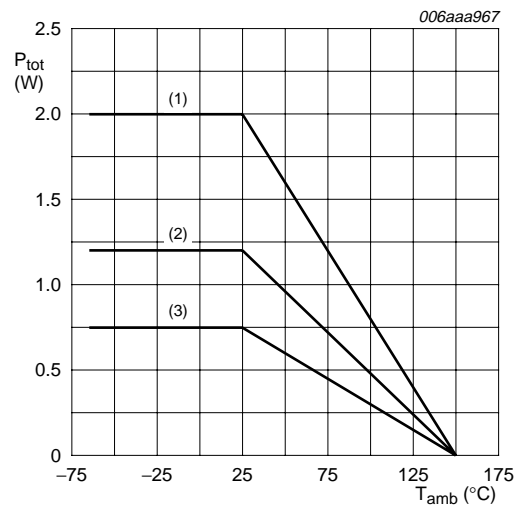
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
Per transistor; for the PNP transistor with negative polarity						
V_{CBO}	collector-base voltage	open emitter	-	50	V	
V_{CEO}	collector-emitter voltage	open base	-	50	V	
V_{EBO}	emitter-base voltage	open collector	-	5	V	
I_C	collector current		-	2.7	A	
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms	-	5	A	
I_B	base current		-	0.5	A	
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	0.55	W
			[2]	-	0.87	W
			[3]	-	1.43	W
Per device						
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	0.75	W
			[2]	-	1.2	W
			[3]	-	2	W
T_j	junction temperature		-	150	°C	
T_{amb}	ambient temperature		-65	+150	°C	
T_{stg}	storage temperature		-65	+150	°C	

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm².

[3] Device mounted on a ceramic PCB, Al₂O₃, standard footprint.



- (1) Ceramic PCB, Al_2O_3 , standard footprint
- (2) FR4 PCB, mounting pad for collector 1 cm^2
- (3) FR4 PCB, standard footprint

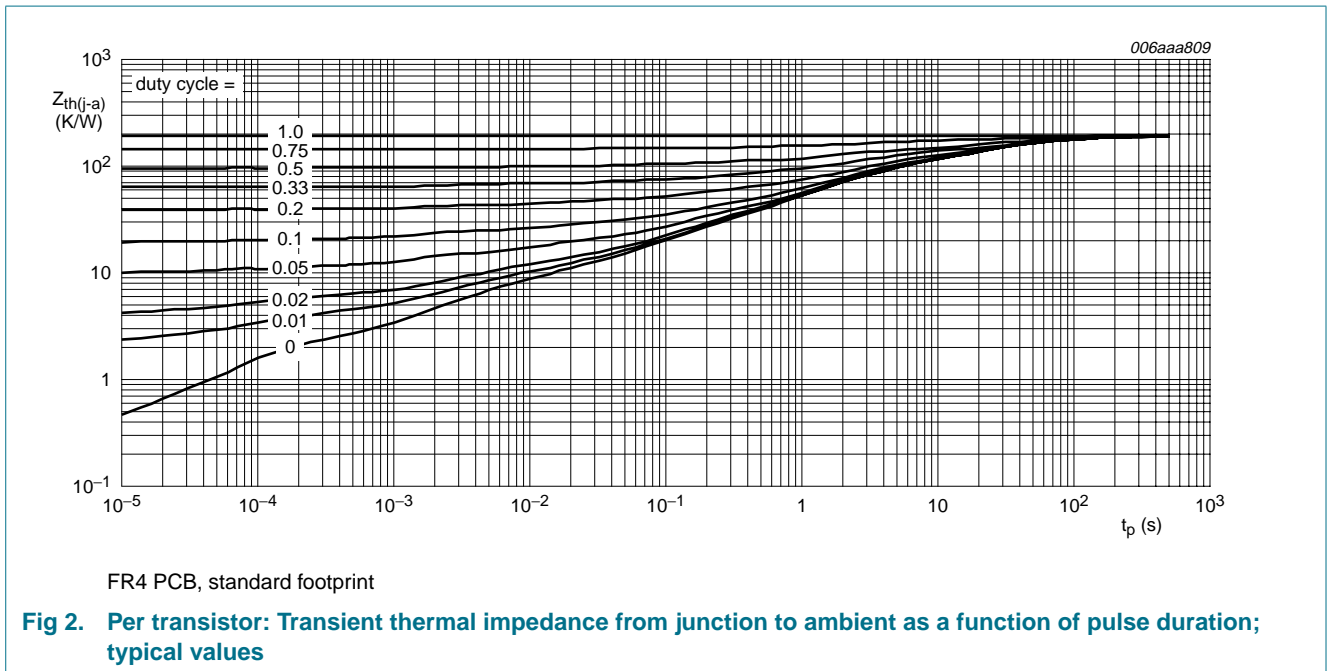
Fig 1. Per device: Power derating curves

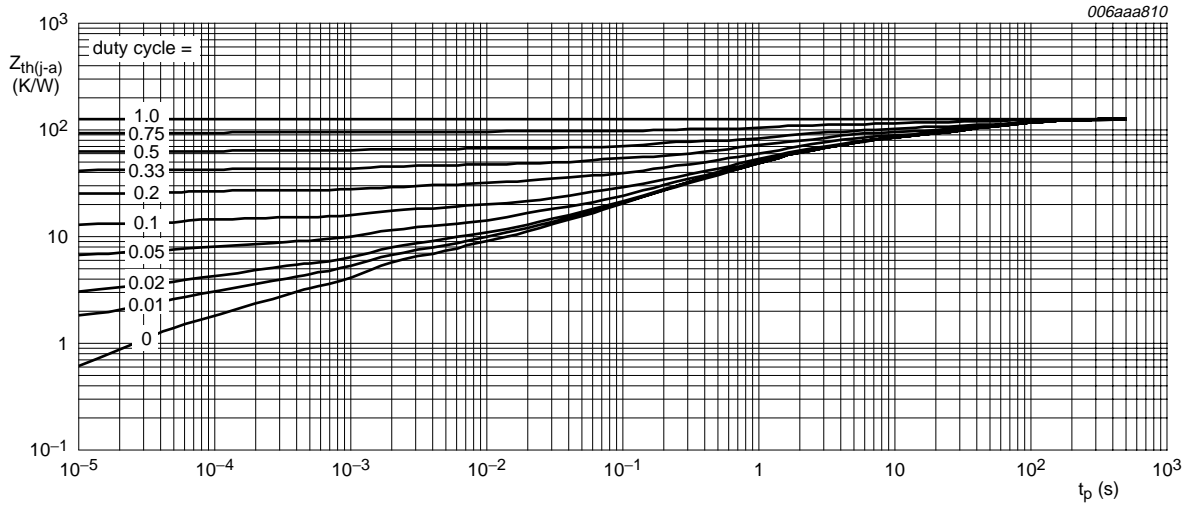
6. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	227	K/W
			[2]	-	144	K/W
			[3]	-	87	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	40	K/W
Per device						
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	167	K/W
			[2]	-	104	K/W
			[3]	-	63	K/W

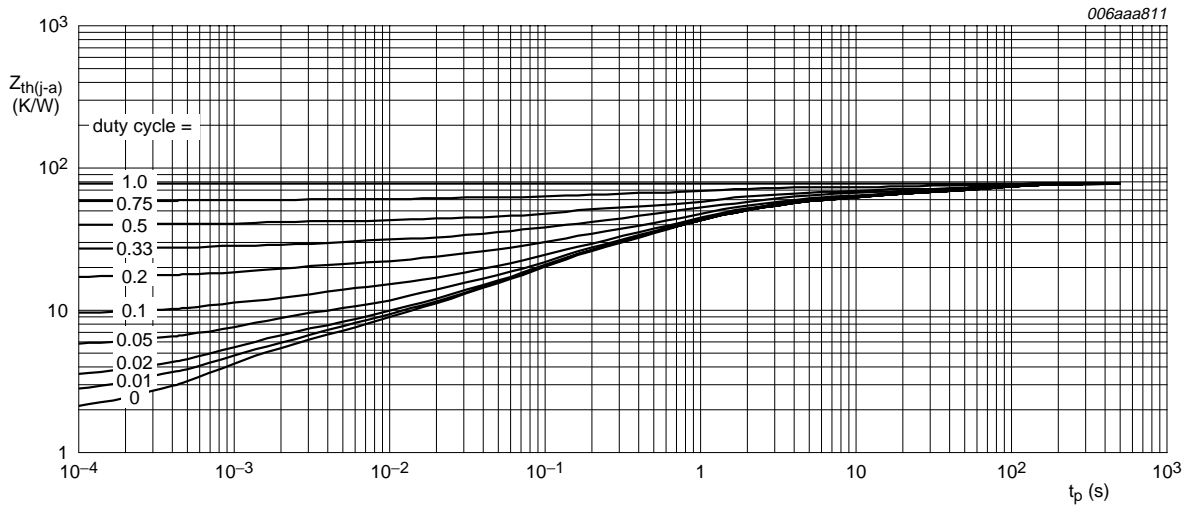
- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm².
- [3] Device mounted on a ceramic PCB, Al₂O₃, standard footprint.





FR4 PCB, mounting pad for collector 1 cm²

Fig 3. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



Ceramic PCB, Al₂O₃, standard footprint

Fig 4. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

7. Characteristics

Table 8. Characteristics

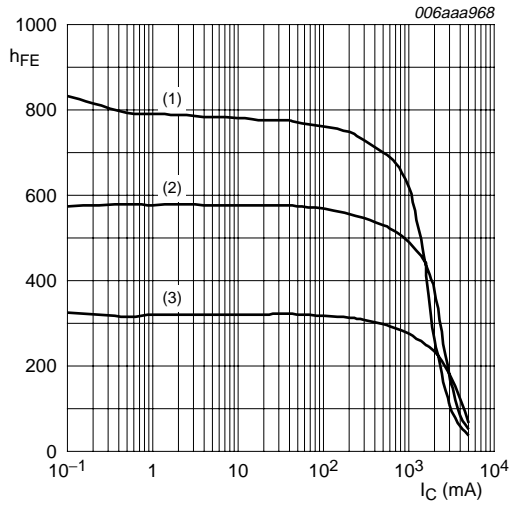
$T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TR1; NPN low V_{CEsat} transistor						
I_{CBO}	collector-base cut-off current	$V_{CB} = 50\text{ V}; I_E = 0\text{ A}$	-	-	100	nA
		$V_{CB} = 50\text{ V}; I_E = 0\text{ A}; T_j = 150\text{ }^{\circ}\text{C}$	-	-	50	μA
I_{CES}	collector-emitter cut-off current	$V_{CE} = 50\text{ V}; V_{BE} = 0\text{ V}$	-	-	100	nA
I_{EBO}	emitter-base cut-off current	$V_{EB} = 5\text{ V}; I_C = 0\text{ A}$	-	-	100	nA
h_{FE}	DC current gain	$V_{CE} = 2\text{ V}; I_C = 100\text{ mA}$	300	520	-	
		$V_{CE} = 2\text{ V}; I_C = 500\text{ mA}$	[1] 300	500	-	
		$V_{CE} = 2\text{ V}; I_C = 1\text{ A}$	[1] 300	470	-	
		$V_{CE} = 2\text{ V}; I_C = 2\text{ A}$	[1] 200	340	-	
		$V_{CE} = 2\text{ V}; I_C = 2.7\text{ A}$	[1] 120	180	-	
V_{CEsat}	collector-emitter saturation voltage		[1]			
		$I_C = 0.5\text{ A}; I_B = 50\text{ mA}$	-	50	80	mV
		$I_C = 1\text{ A}; I_B = 50\text{ mA}$	-	100	160	mV
		$I_C = 2\text{ A}; I_B = 100\text{ mA}$	-	190	280	mV
		$I_C = 2\text{ A}; I_B = 200\text{ mA}$	-	180	260	mV
		$I_C = 2.7\text{ A}; I_B = 270\text{ mA}$	-	240	340	mV
R_{CEsat}	collector-emitter saturation resistance	$I_C = 2\text{ A}; I_B = 200\text{ mA}$	[1] -	90	130	$\text{m}\Omega$
			[1]			
V_{BEsat}	base-emitter saturation voltage		[1]			
		$I_C = 2\text{ A}; I_B = 100\text{ mA}$	-	0.95	1.1	V
		$I_C = 2.7\text{ A}; I_B = 270\text{ mA}$	-	1.1	1.2	V
V_{BEon}	base-emitter turn-on voltage	$V_{CE} = 2\text{ V}; I_C = 1\text{ A}$	[1] -	0.8	1.2	V
t_d	delay time	$V_{CC} = 10\text{ V}; I_C = 2\text{ A}; I_{Bon} = 100\text{ mA}; I_{Boff} = -100\text{ mA}$	-	8	-	ns
t_r	rise time		-	96	-	ns
t_{on}	turn-on time		-	104	-	ns
t_s	storage time		-	355	-	ns
t_f	fall time		-	165	-	ns
t_{off}	turn-off time		-	520	-	ns
C_c	collector capacitance	$V_{CB} = 10\text{ V}; I_E = i_e = 0\text{ A}; f = 1\text{ MHz}$	-	18	25	pF

Table 8. Characteristics ...continued $T_{amb} = 25^\circ\text{C}$ unless otherwise specified.

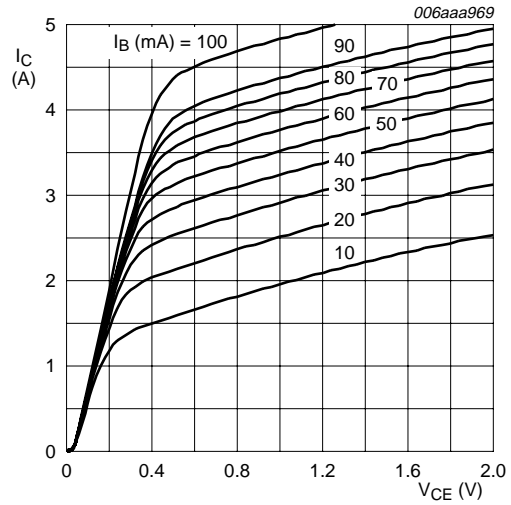
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TR2; PNP low V_{CEsat} transistor						
I_{CBO}	collector-base cut-off current	$V_{CB} = -50\text{ V}; I_E = 0\text{ A}$	-	-	-100	nA
		$V_{CB} = -50\text{ V}; I_E = 0\text{ A}; T_j = 150^\circ\text{C}$	-	-	-50	μA
I_{CES}	collector-emitter cut-off current	$V_{CE} = -50\text{ V}; V_{BE} = 0\text{ V}$	-	-	-100	nA
I_{EBO}	emitter-base cut-off current	$V_{EB} = -5\text{ V}; I_C = 0\text{ A}$	-	-	-100	nA
h_{FE}	DC current gain	$V_{CE} = -2\text{ V}; I_C = -100\text{ mA}$	200	340	-	
		$V_{CE} = -2\text{ V}; I_C = -500\text{ mA}$	[1] 200	290	-	
		$V_{CE} = -2\text{ V}; I_C = -1\text{ A}$	[1] 180	250	-	
		$V_{CE} = -2\text{ V}; I_C = -2\text{ A}$	[1] 130	180	-	
		$V_{CE} = -2\text{ V}; I_C = -2.7\text{ A}$	[1] 95	135	-	
V_{CEsat}	collector-emitter saturation voltage		[1]			
		$I_C = -0.5\text{ A}; I_B = -50\text{ mA}$	-	-60	-90	mV
		$I_C = -1\text{ A}; I_B = -50\text{ mA}$	-	-125	-180	mV
		$I_C = -2\text{ A}; I_B = -100\text{ mA}$	-	-225	-320	mV
		$I_C = -2\text{ A}; I_B = -200\text{ mA}$	-	-190	-280	mV
	$I_C = -2.7\text{ A}; I_B = -270\text{ mA}$	-	-255	-370	mV	
R_{CEsat}	collector-emitter saturation resistance	$I_C = -2\text{ A}; I_B = -200\text{ mA}$	[1] -	95	140	$\text{m}\Omega$
V_{BEsat}	base-emitter saturation voltage		[1]			
		$I_C = -2\text{ A}; I_B = -100\text{ mA}$	-	-0.95	-1.1	V
		$I_C = -2.7\text{ A}; I_B = -270\text{ mA}$	-	-1	-1.2	V
V_{BEon}	base-emitter turn-on voltage	$V_{CE} = -2\text{ V}; I_C = -1\text{ A}$	[1] -	-0.8	-1.2	V
t_d	delay time	$V_{CC} = -10\text{ V}; I_C = -2\text{ A};$	-	9	-	ns
t_r	rise time	$I_{Bon} = -100\text{ mA};$	-	54	-	ns
t_{on}	turn-on time	$I_{Boff} = 100\text{ mA}$	-	63	-	ns
t_s	storage time		-	190	-	ns
t_f	fall time		-	50	-	ns
t_{off}	turn-off time		-	240	-	ns
C_c	collector capacitance	$V_{CB} = -10\text{ V}; I_E = I_C = 0\text{ A};$ $f = 1\text{ MHz}$	-	25	35	pF

[1] Pulse test: $t_p \leq 300\ \mu\text{s}; \delta \leq 0.02$.



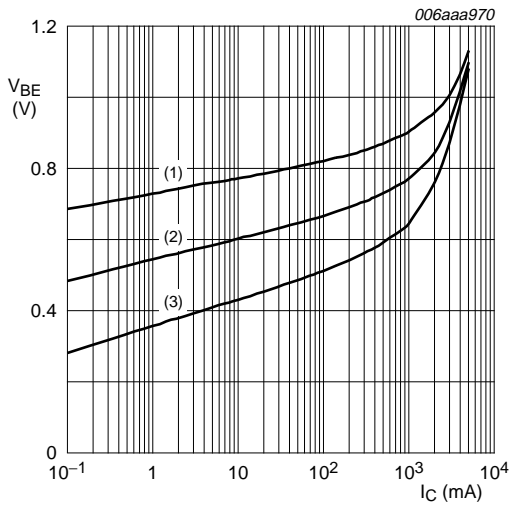
$V_{CE} = 2\text{ V}$
 (1) $T_{amb} = 100\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = -55\text{ °C}$

Fig 5. TR1 (NPN): DC current gain as a function of collector current; typical values



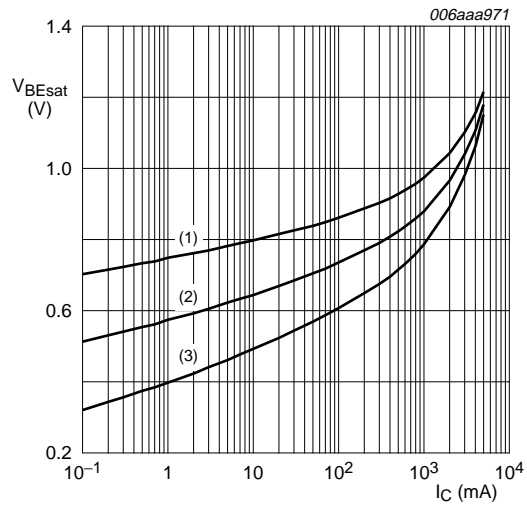
$T_{amb} = 25\text{ °C}$

Fig 6. TR1 (NPN): Collector current as a function of collector-emitter voltage; typical values



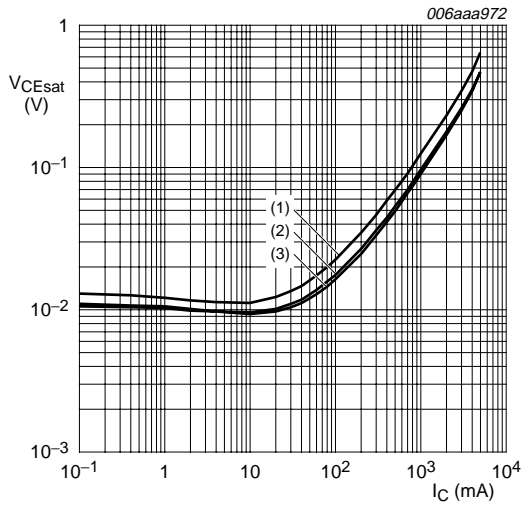
$V_{CE} = 2\text{ V}$
 (1) $T_{amb} = -55\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = 100\text{ °C}$

Fig 7. TR1 (NPN): Base-emitter voltage as a function of collector current; typical values



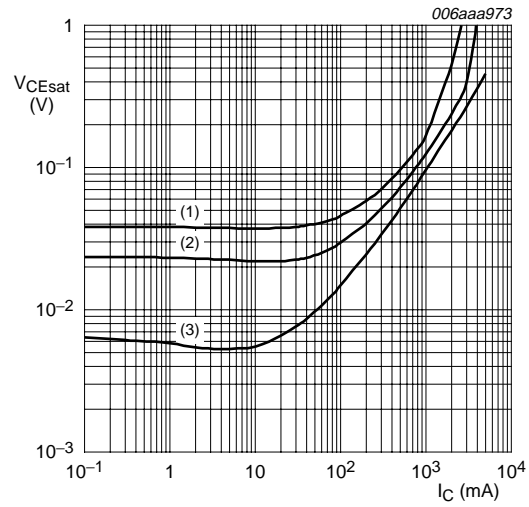
$I_C/I_B = 20$
 (1) $T_{amb} = -55\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = 100\text{ °C}$

Fig 8. TR1 (NPN): Base-emitter saturation voltage as a function of collector current; typical values



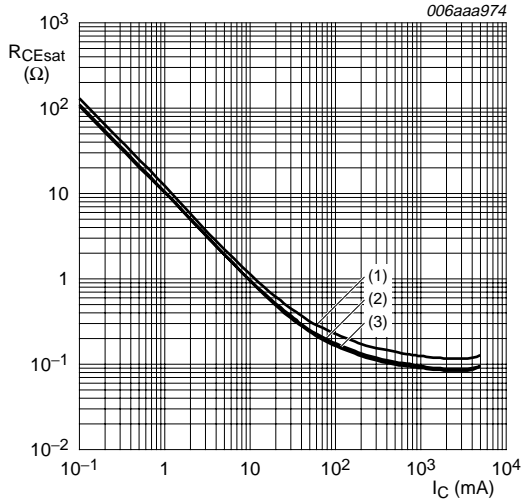
$I_C/I_B = 20$
 (1) $T_{amb} = 100\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = -55\text{ °C}$

Fig 9. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values



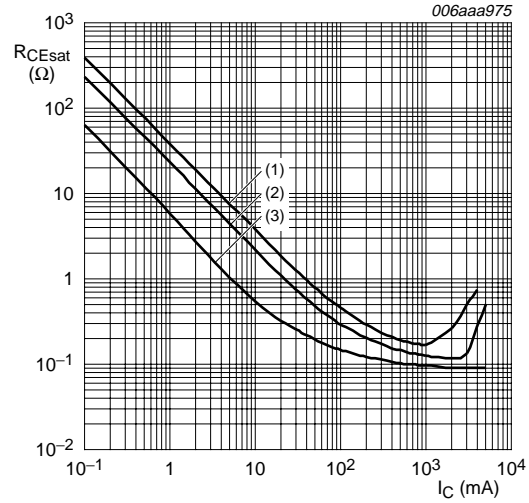
$T_{amb} = 25\text{ °C}$
 (1) $I_C/I_B = 100$
 (2) $I_C/I_B = 50$
 (3) $I_C/I_B = 10$

Fig 10. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values



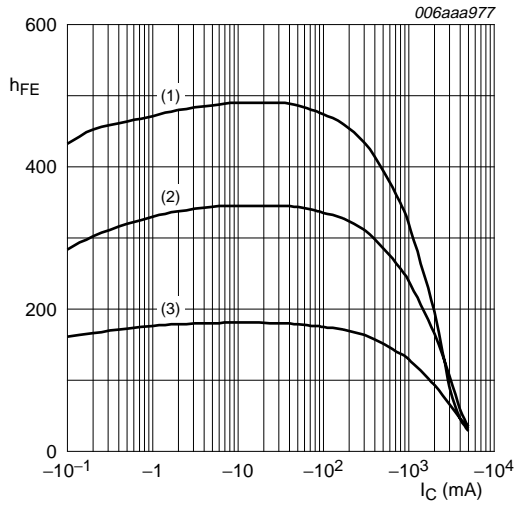
$I_C/I_B = 20$
 (1) $T_{amb} = 100\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = -55\text{ °C}$

Fig 11. TR1 (NPN): Collector-emitter saturation resistance as a function of collector current; typical values



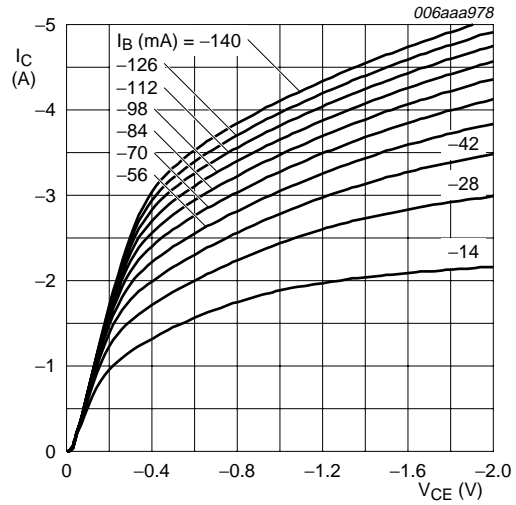
$T_{amb} = 25\text{ °C}$
 (1) $I_C/I_B = 100$
 (2) $I_C/I_B = 50$
 (3) $I_C/I_B = 10$

Fig 12. TR1 (NPN): Collector-emitter saturation resistance as a function of collector current; typical values



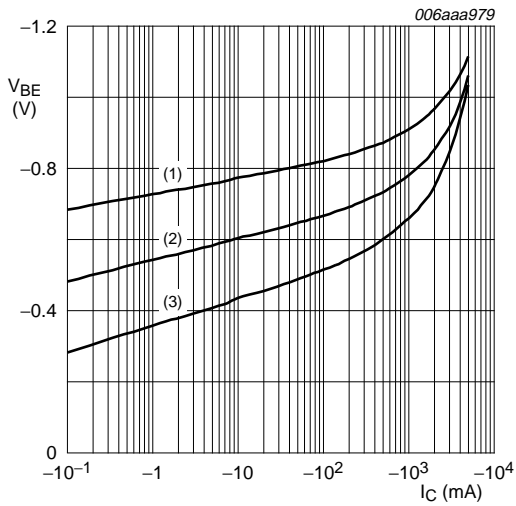
$V_{CE} = -2\text{ V}$
 (1) $T_{amb} = 100\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = -55\text{ °C}$

Fig 13. TR2 (PNP): DC current gain as a function of collector current; typical values



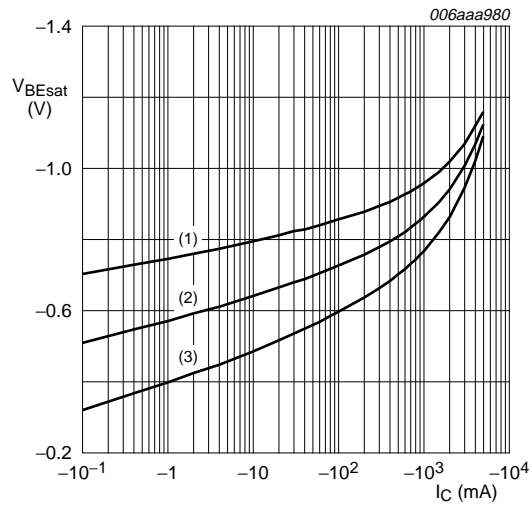
$T_{amb} = 25\text{ °C}$

Fig 14. TR2 (PNP): Collector current as a function of collector-emitter voltage; typical values



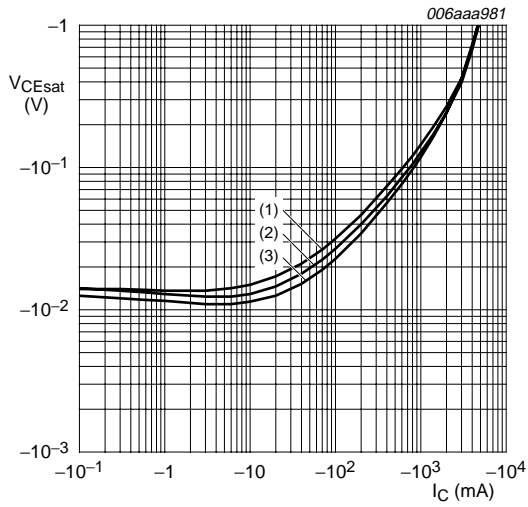
$V_{CE} = -2\text{ V}$
 (1) $T_{amb} = -55\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = 100\text{ °C}$

Fig 15. TR2 (PNP): Base-emitter voltage as a function of collector current; typical values



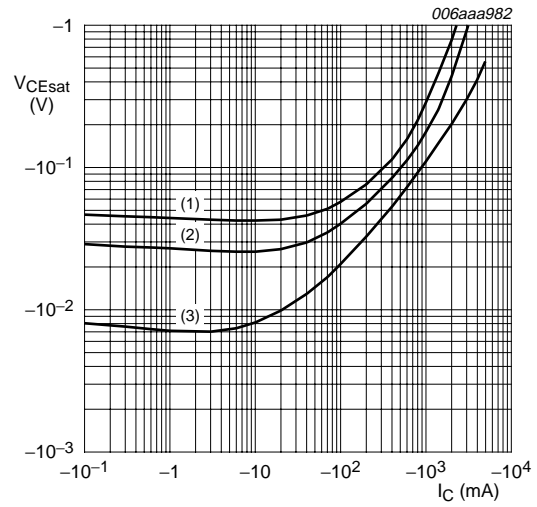
$I_C/I_B = 20$
 (1) $T_{amb} = -55\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = 100\text{ °C}$

Fig 16. TR2 (PNP): Base-emitter saturation voltage as a function of collector current; typical values



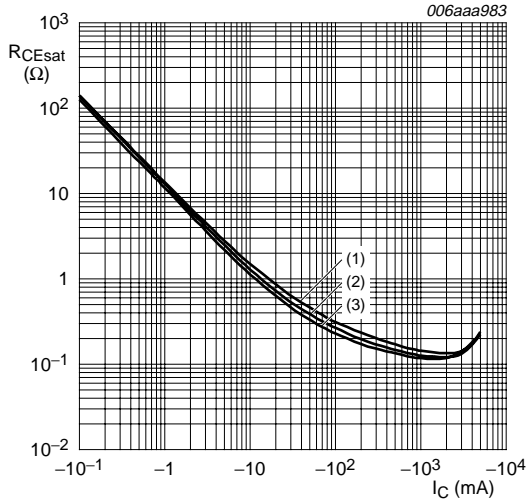
$I_C/I_B = 20$
 (1) $T_{amb} = 100\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = -55\text{ °C}$

Fig 17. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values



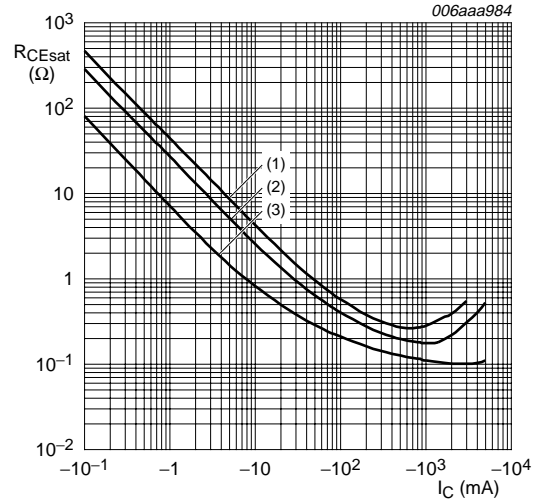
$T_{amb} = 25\text{ °C}$
 (1) $I_C/I_B = 100$
 (2) $I_C/I_B = 50$
 (3) $I_C/I_B = 10$

Fig 18. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values



$I_C/I_B = 20$
 (1) $T_{amb} = 100\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = -55\text{ °C}$

Fig 19. TR2 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values



$T_{amb} = 25\text{ °C}$
 (1) $I_C/I_B = 100$
 (2) $I_C/I_B = 50$
 (3) $I_C/I_B = 10$

Fig 20. TR2 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values

8. Test information

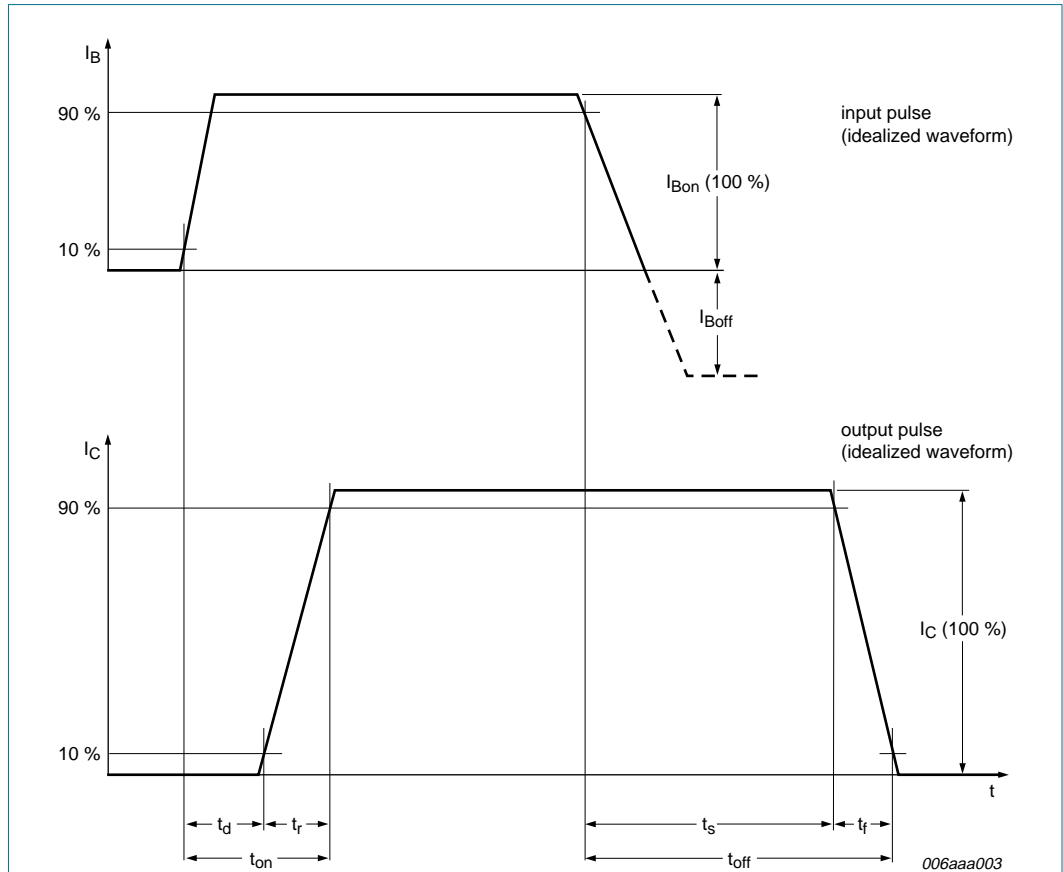


Fig 21. TR1 (NPN): BISS transistor switching time definition

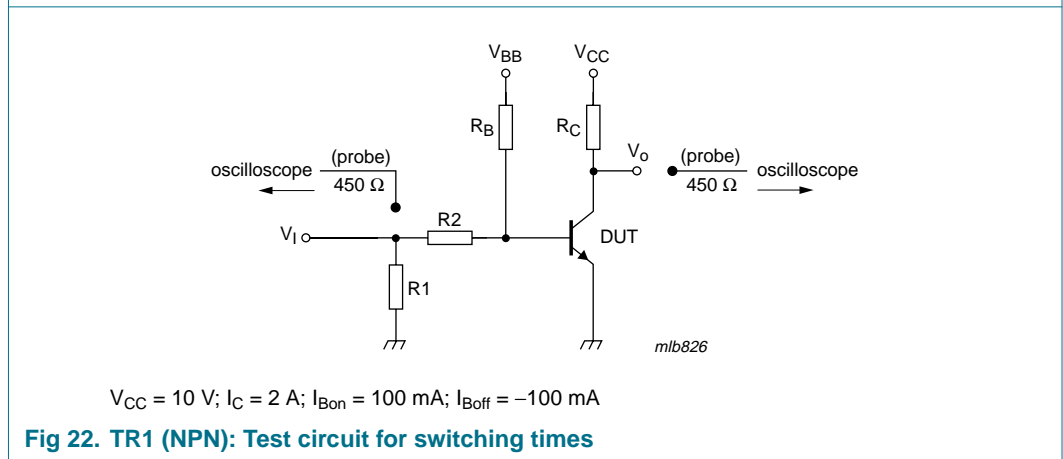


Fig 22. TR1 (NPN): Test circuit for switching times

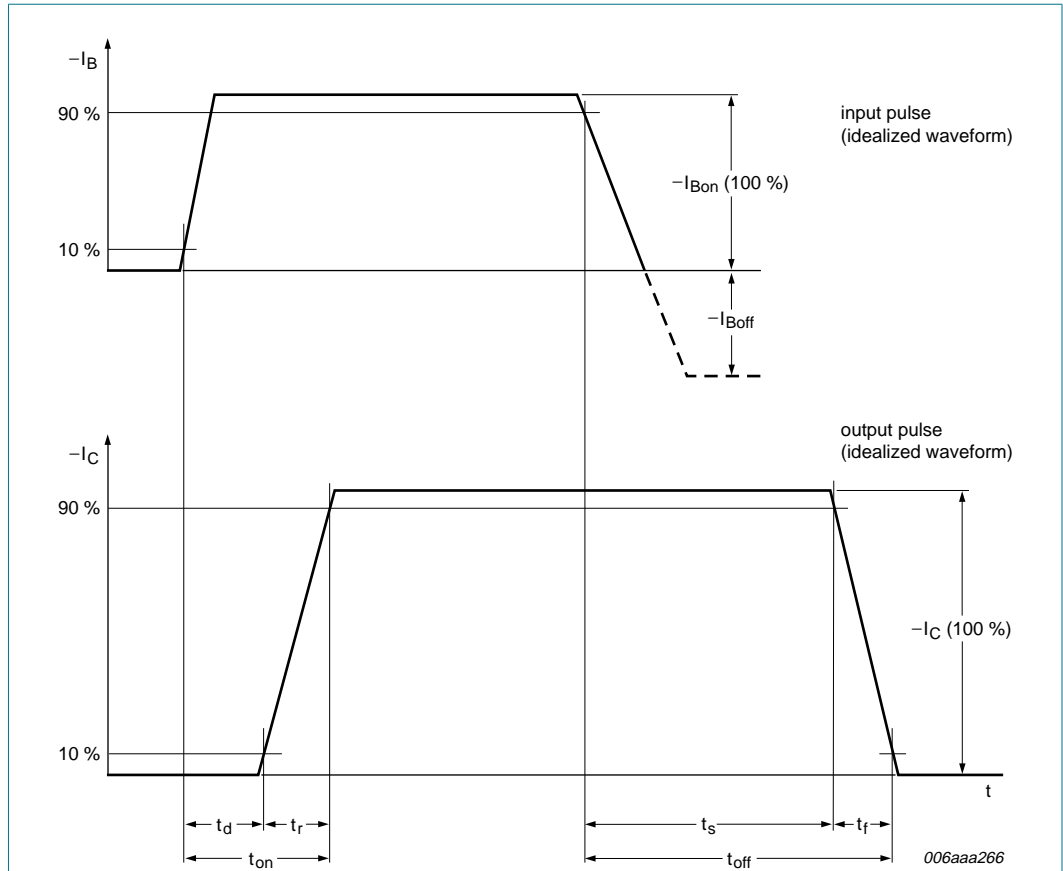


Fig 23. TR2 (PNP): BISS transistor switching time definition

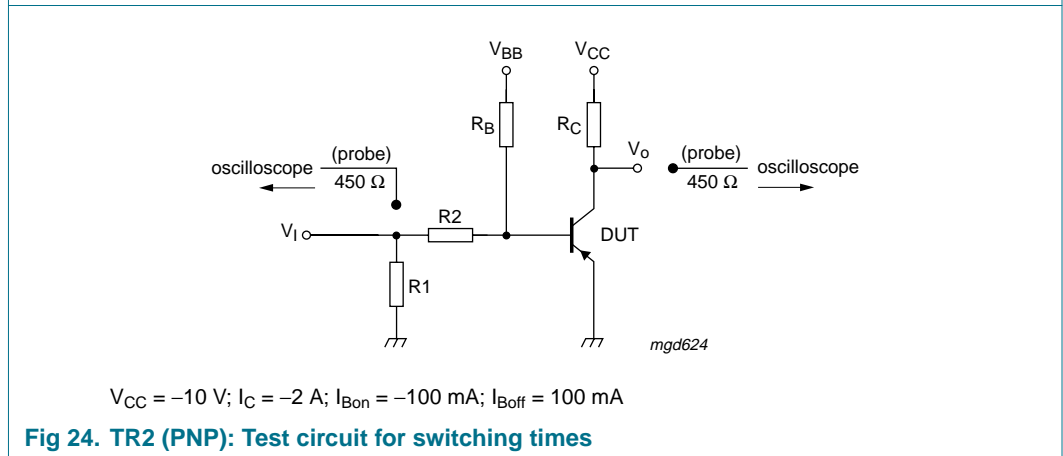
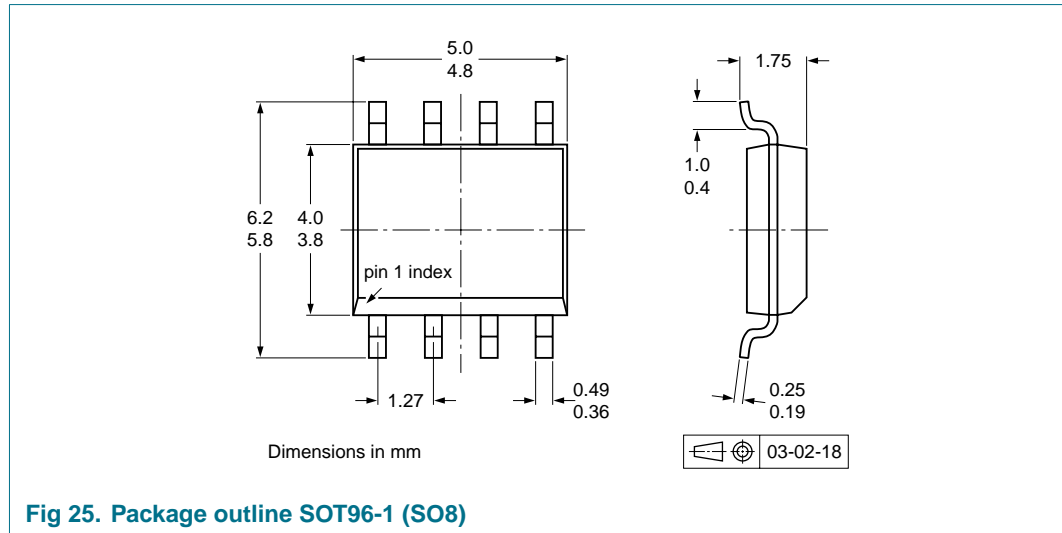


Fig 24. TR2 (PNP): Test circuit for switching times

9. Package outline



10. Packing information

Table 9. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.^[1]

Type number	Package	Description	Packing quantity	
			1000	2500
PBSS4350SPN	SOT96-1	8 mm pitch, 12 mm tape and reel	-115	-118

[1] For further information and the availability of packing methods, see [Section 14](#).

11. Soldering

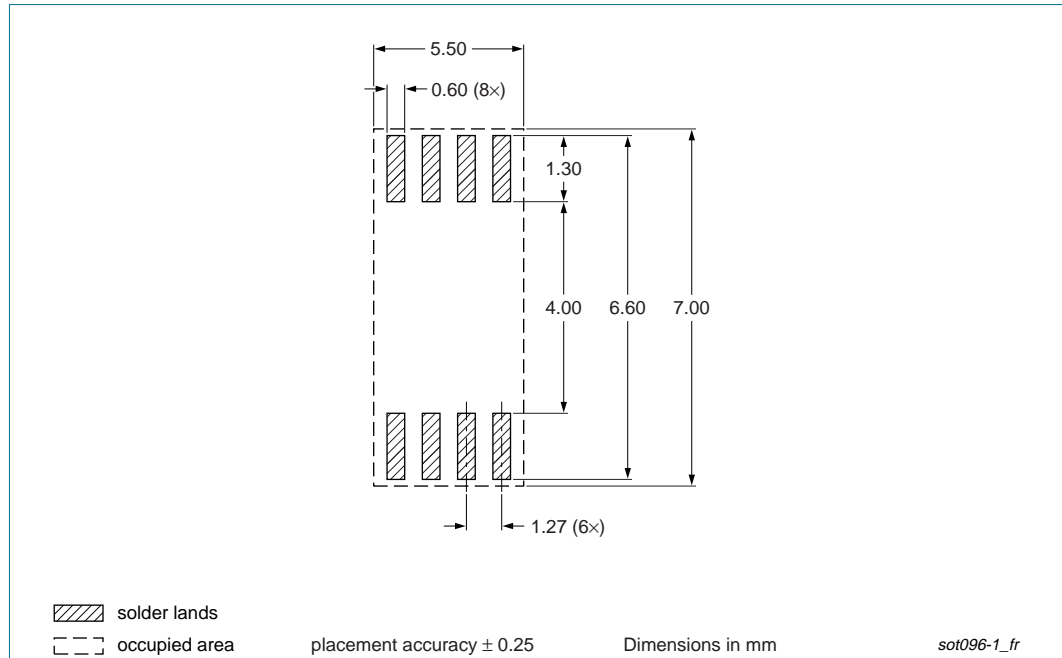


Fig 26. Reflow soldering footprint SOT96-1 (SO8)

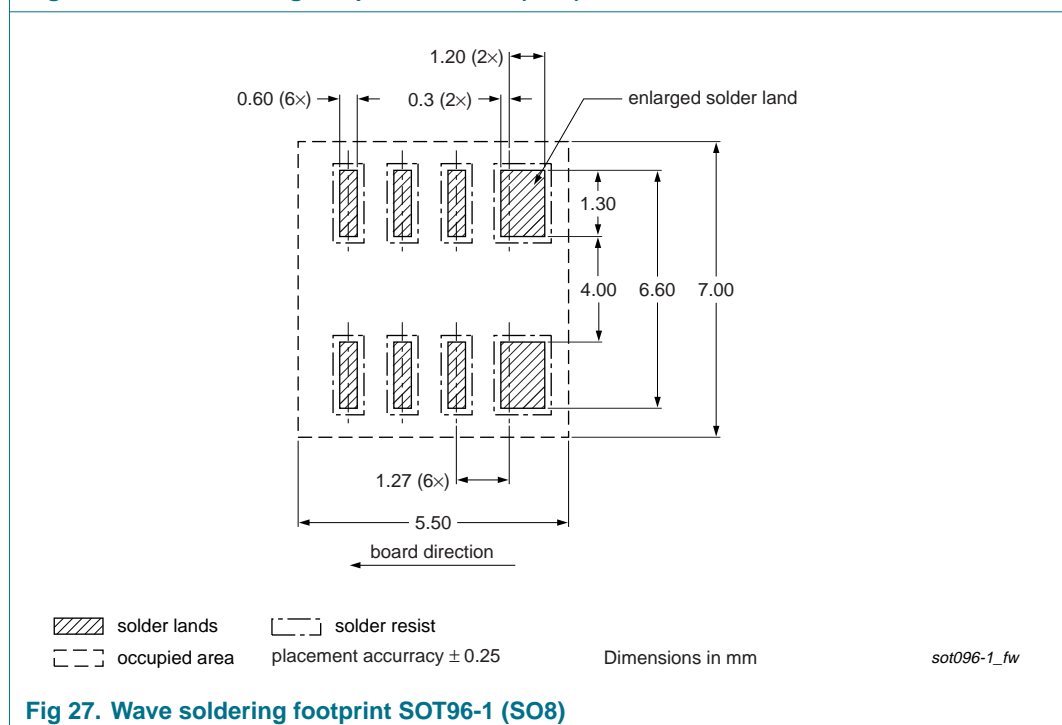


Fig 27. Wave soldering footprint SOT96-1 (SO8)

12. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PBSS4350SPN_1	20070405	Product data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

13.2 Definitions

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15. Contents

1	Product profile	1
1.1	General description	1
1.2	Features	1
1.3	Applications	1
1.4	Quick reference data	1
2	Pinning information	2
3	Ordering information	2
4	Marking	2
5	Limiting values	3
6	Thermal characteristics	5
7	Characteristics	7
8	Test information	13
9	Package outline	15
10	Packing information	15
11	Soldering	16
12	Revision history	17
13	Legal information	18
13.1	Data sheet status	18
13.2	Definitions	18
13.3	Disclaimers	18
13.4	Trademarks	18
14	Contact information	18
15	Contents	19